



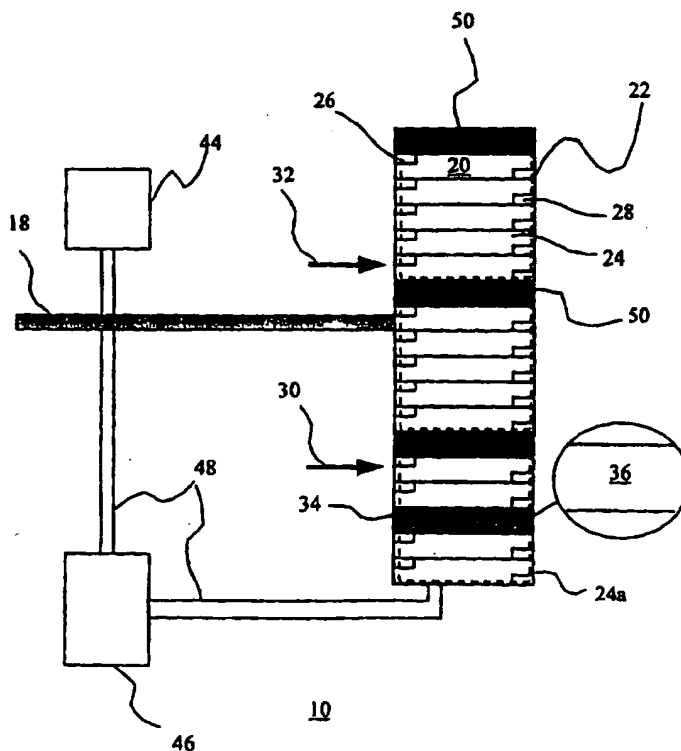
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(54) Title: MEMORY DEVICES

(57) Abstract

A computer system has a memory device comprising a user interface, a controller, a store, and address mapping means for mapping a first address from the user interface to a second address for accessing the store, where the controller stores information in successive regions of the store each time the information is updated.



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Memory Devices

The present invention relates to memory devices. It finds particular application in the field of magnetic disk drive emulation.

Non-volatile memories are frequently used in semiconductor applications because they store information without the need for power to be applied to the memory. In particular, non-volatile memories are used as solid state storage devices for emulating magnetic disks.

European Patent Application No. 0615184A2 (IBM) shows a FLASH memory filing system which is protected against block and device failures by storing data in duplicate and using a redundancy area in each logical block in association with error correction codes. Cluster management information is stored in headers which are written in duplicate to two physical blocks. Included in this information is an erase counter to ensure that the physical limit for a block is not exceeded.

One type of non-volatile memory commonly used for disk drive emulation is FLASH EPROM. FLASH EPROM has a number of peculiar characteristics. For example, data can only be written to a location which has previously been erased. Individual locations cannot be erased, the memory must be bulk erased in units of an erasable block. Permanent failure of the cell may result from too many write/erase cycles. Typically, the total number of times that a location may be erased and written is limited to the range 100,000 to 1,000,000 cycles.

There are certain characteristics of solid state disk memories that use FLASH EPROM. The memory medium must be bulk erased in units of an erasable block which is normally greater than the size of a data block (also known as a sector). Since a cell of FLASH EPROM cannot be modified without an erase operation being performed first, rewriting of a sector must occur in a different physical location causing the contents of its previous location to become obsolete.

Data transferred to a memory system from a host is termed a logical sector and it corresponds to a logical address. This logical address is translated by the memory system to a physical address which addresses a physical location in the memory.

Sectors in the memory which contain valid data must be relocated from an erasable block before the block can be erased to recover memory space occupied by obsolete sectors.

The physical location allocated to a logical sector address is variable, that is, a physical location will not always correspond to one particular logical address. Therefore, the physical locations that correspond to the logical addresses must be stored in a lookup table or a similar device to record the logical to physical address mappings. The algorithms used
5 for writing sector data to the memory medium and for erasing the memory medium must ensure uniform utilisation of the medium and elimination of any memory "hot-spots" and wear-out effects.

Information must be stored in a non-volatile memory to allow the control system for the solid state storage device which is emulating the magnetic disk to be correctly
10 initialised after electrical power has been removed and then restored. This information (the control information) includes memory address pointers which must be known to re-establish correctly the algorithms for erasing or writing. Status information relating to execution of critical operations such as the relocation of blocks of data within the memory system is also included in the control information.

15 Storage of control information presents no problem for magnetic disks because a full directory for locating files and sectors on a disk can be located at a known physical location on the disk. Data within this directory can be modified and rewritten at the same physical location. A magnetic disk does not require bulk erasure of the storage medium before data can be written. Neither is there any hazard to the reliability of the disk by
20 repeatedly writing and erasing the same location.

However, storage of control information is a problem for non-byte erasable memory because the information must be in a physical location which can be located by the control system after electrical power has been removed and then restored. Control information cannot be updated in a fixed physical location without bulk erasure of the memory medium.
25 but the number of erase/write cycles which can be applied to control information at a fixed physical location is restricted by the limited endurance characteristics of the technology. The limited write/erase cycle endurance of FLASH EPROM technology is particularly acute.

Previous teaching is that the solution to the problem of having to modify the control
30 information frequently on a block erasable memory lies in storing the control information in a different location each time it is written. This, however, has a number of serious

problems associated with it. If power is unexpectedly lost because of a power cut or accidental removal of the memory from the host then the system would have no way of locating the control information necessary for operating the system because it would be stored in a random place.

5 The present invention is therefore concerned with repeatedly storing information in different locations in memory while ensuring that in the event of an unexpected power loss the said information can be recovered.

According to the present invention there is provided a memory device comprising a user interface, a controller, a store, and address mapping means for mapping a first
10 address from the user interface to a second address for accessing the store, where the controller stores information in successive regions of the store each time the information is updated.

For a better understanding of the present invention and to show how the same may be carried into effect, reference will now be made, by way of example to the accompanying
15 diagrams in which:

Figure 1 shows a memory system based on the present invention;

Figure 2 shows a diagram of the logical to physical translation table associated with the FLASH memory;

Figure 3 shows the format of the logical address for each block header; and

20 Figure 4 shows the format of the pointer control sector.

Referring to Figure 1, this shows a memory system 10 with a user interface 18 for transferring data between a host and a store. A FLASH memory device 20 is used as the main store. The memory system 10 emulates a solid state disk in a similar way to the system disclosed in UK patent application 9519670.5. FLASH storage devices are
25 frequently used for magnetic disk emulation because the physical size of each storage cell is smaller than the physical size of an EEPROM cell.

The FLASH memory device 20 is composed of erase blocks 22. Each erase block 22 is the minimum erasable blocksize. Each erase block 22 is composed of a number of sectors 24. Data is read and written in units of one sector 24 (typically 512 bytes plus
30 header information 26 and error correcting codes 28). Sectors 24 may be stored in the FLASH memory device 20 with a constant blocksize or may have a blocksize which is

variable between sectors 24, such as would result if data compression were applied to the data. Sectors 24 are sometimes closely packed in the memory address space and their locations may not align uniformly with the structure of the erase blocks 22 in the memory. The memory system 10 of the present embodiment has a write pointer 30 to point to the area of memory which is to be written to next, and an erase pointer 32 to point to the area of memory which is to be erased next. Locations which lie between the write pointer 30 and the erase pointer 32 are in the erased state. Erase operations are scheduled to maintain a predetermined number of erased locations between the write pointer 30 and the erase pointer 32. Sectors 24 containing valid data which are located within an erase block 22 scheduled for erasure are first relocated one at a time to the location defined by the write pointer 30. The write pointer 30 and the erase pointer 32 are incremented after the write and erase operations respectively, and continuously cycle incrementally through the entire physical memory space. The erase/write algorithm automatically ensures the frequency of erasing and writing to the physical memory is equalised throughout the entire memory space.

The present invention could apply equally to any memory system which controls the cumulative number of erase/write cycles at a memory location.

In one embodiment of the present invention a single control sector 34 is used to record the control information 36 for the entire FLASH memory 20. The control information 36 contains the present location of the write pointer 30, the erase pointer 32, and additional status information which may vary depending on the particular application. The control information 36 is stored at a fixed location in logical address space rather than a fixed location in physical address space.

The control information 36 is stored at a location which cannot be accessed by the host. In this embodiment of the present invention the control information 36 is stored at the highest available logical address 38 and the host is only given an addressable range 40 from the lowest logical address up to the start of the control sector address. Thus the control information 36 is inaccessible by the host.

The control sector 34 has a fixed logical address but the physical location of the control sector 34 changes each time it is written. The current control sector physical address 42 is found by accessing the highest available logical address 38 in the logical to

physical translation table 44 (which could be a lookup table).

The control sector physical address 42 is determined by an identical logical to physical address translation process to that used for data sectors 24 which are accessible by the host.

5 The control information 36 in the control sector 34 is rewritten regularly under the supervision of a controller 46, which controls the FLASH memory 20 and the logical to physical translation table 44 with control lines 48. The controller 46 ensures that every significant change in the control information 36 is rewritten.

10 The size of a control sector 34 containing control information 36 need not be the same as that of a sector 24 containing host data, but may be only as large as necessary to contain the control information 36. A control sector 34 contains header information 26 and error correcting codes 28 in identical format to those in a sector containing host data.

When any sector 24 is written to FLASH memory 20, its physical sector address location is defined by the current write pointer 30. The control sector physical address 42 (that is, the logical to physical translation table entry for the control information's logical address) therefore contains the value of the write pointer 30 at the time the sector 24 containing the control information 36 was written. Therefore, in some embodiments of this invention the value of the write pointer 30 may be derived from the control sector physical address 42 rather than being stored explicitly as a control information 36 entry. If the control information 36 is rewritten regularly then the physical sector address stored in the control information 36 is always slightly less than or equal to the current write pointer 30. Each sector 24 has a sector header which contains a write flag which is set when data is written to the sector 24. The value of the write pointer 30 can be determined during device initialisation by reading the control sector physical address 42 from the logical to physical translation table 44. Successive sector headers are then read, starting from the control sector physical address 42 read from the logical to physical translation table 44 until the first header is found with the write flag cleared. The current write pointer 30 is this address of the first header with its write flag cleared. The control information 36 will be rewritten whenever the erase pointer 32 is incremented, that is, each time an erase block operation takes place. An erase block 22 is the minimum area that can be independently erased in the FLASH memory 20 and may contain a number of sectors 24, as shown in Figure 1.

Where there is a large volume of control information 36, it may be beneficial to include multiple control sectors 34 in the system. Each of the multiple control sectors 34 would contain different parts of the control information 36 and each with a unique logical address which is inaccessible to the host.

5 Using multiple control sectors 34 minimises the amount of erased memory capacity which is consumed when control information 36 has to be rewritten following a change in its contents. For example, in one embodiment of the above memory system 10, control information 36 is stored about each individual erasable block. It is necessary to define the address of the first sector 24a within the erasable block 22 because sectors 24 are closely
10 packed and do not align with the boundaries between erasable blocks 22. With the address of the first sector 24a defined, valid sectors can be located within the erase block 22 and relocated prior to an erase operation on the block 22. The address of the first sector 24a can be marked by writing a unique control sector 34 as the first sector 24a in each erasable block 22.

15 In the present embodiment the control information 36 for each erase block 22 is included in each block 22 as a block header 50. Each block header 50 is very small, only containing enough bytes for essential information. The block headers 50 are all located in a logical address space which is not accessible by the host, but which is accessible by the controller 46. The highest available logical address 38 in this embodiment is a range of
20 addresses, all of which are inaccessible by the host.

Block headers 50 are located in FLASH memory 20 and are addressed by way of a logical to physical translation table 44 in the same way as any other sector 24. The logical address for each block header 50 is formed by a descriptor field 52 composed of two parts, as shown in Figure 3. The first part of the descriptor field 52 is a block header
25 identifier 54 which is the same for each block header 50. The second part of the descriptor field 52 relates to the particular erase block number 56.

Other block headers 50 may also exist which contain different information and have different identifiers in their logical sector address. For example, a pointer control sector 58 may exist for storing the value of the erase pointer 32. The pointer control sector 58 will
30 be written immediately after an erase block 22 has been erased. The logical to physical translation table entry for the pointer control sector 58 contains a pointer physical address

60 which is the value of the write pointer 30 which existed at the time the pointer control sector 58 was written. The current value of the write pointer 30 will lie within a range of approximately one erase block 22 above this pointer physical address 60.

It will be appreciated that various modifications may be made to the above described embodiment within the ambit of the present invention. For example, the store
5 may be any block erasable memory, not merely a semiconductor memory.

Claims

1. A memory device comprising a user interface (18), a controller (46), a store (), and address mapping means (44) for mapping a first address from the user interface to a second address for accessing the store **characterised in that** the controller stores control
5 information in successive regions of the store each time the information is updated.
2. A memory device according to claim 1 **characterised in that** the control information comprises the current positions of a write pointer (30) and an erase pointer (32).
3. A memory device according to claim 1 or claim 2 **characterised in that** said control information is stored at a fixed location in logical address space.
- 10 4. A memory device according to claim 3 **characterised in that** logical locations at which said control information is stored are barred from access by the host.
5. A memory device according to claim 4 **characterised in that** control information (36) is stored at the highest available logical address (38) and the host is only given an addressable range (40) from the lowest logical address up to the start of the control sector
15 address.
6. A memory device according to any one of the preceding claims **characterised in that** said address mapping means (44) maintains a constant first address for the said information.

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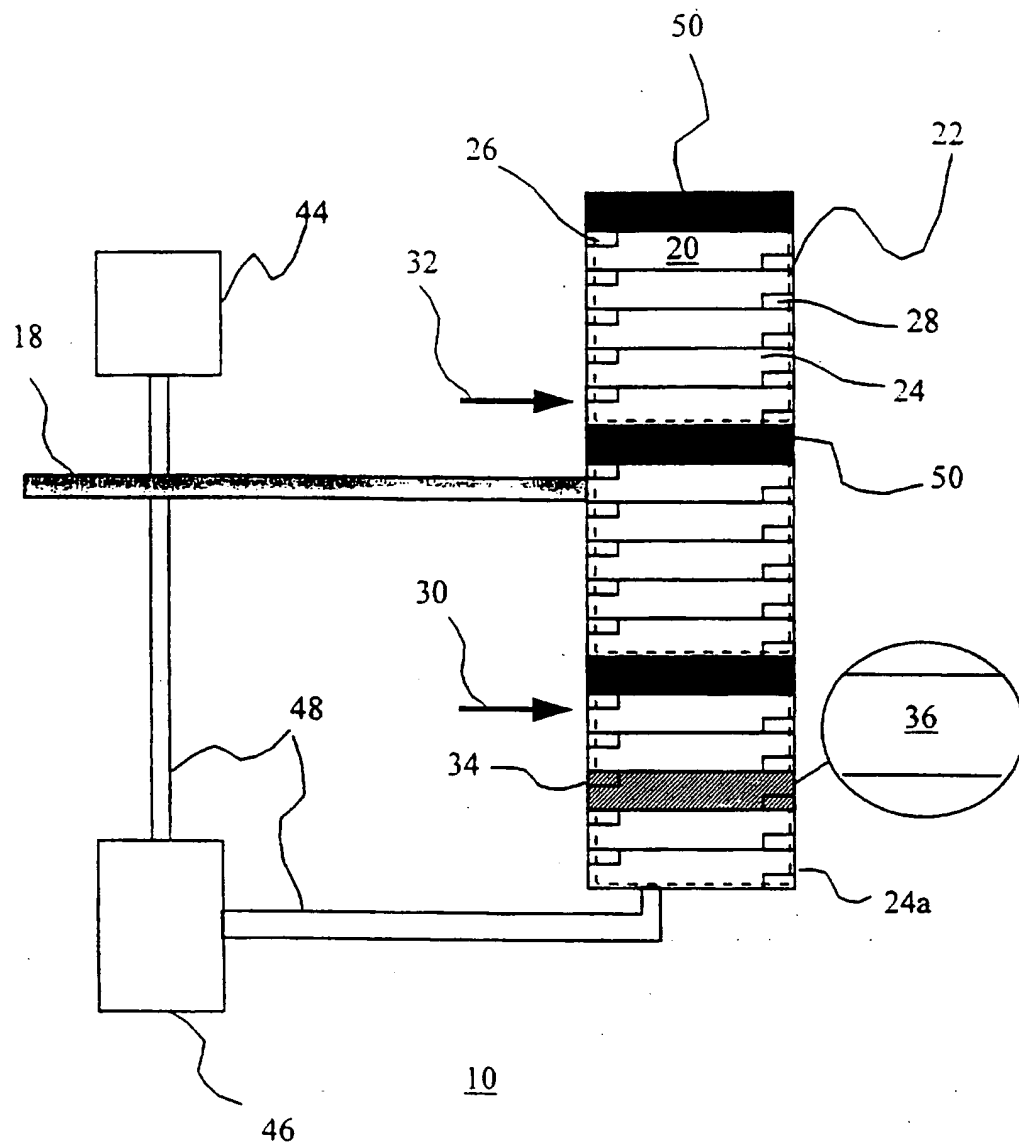


Figure 1

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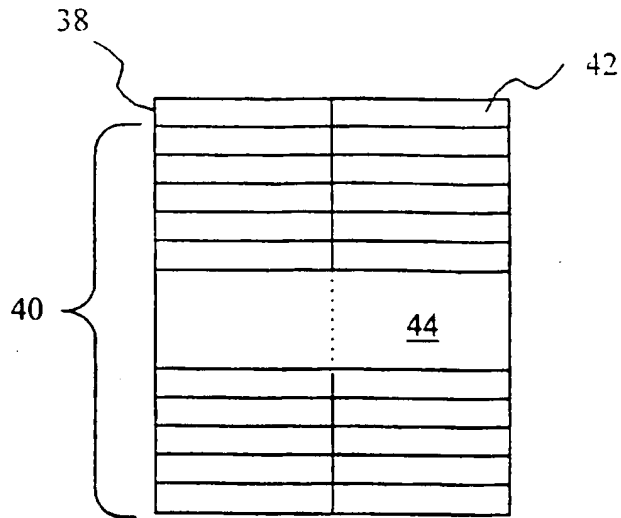
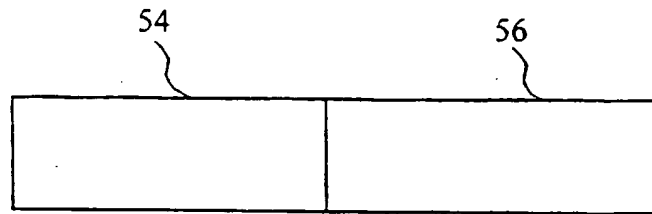
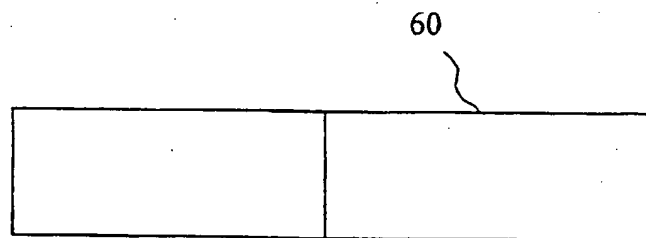


Figure 2



52

Figure 3



58

Figure 4

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 97/00934

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F3/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 291 991 A (MEMORY CORP PLC) 7 February 1996 cited in the application see figures 1,3A,3B see page 3, line 29 - page 5, line 8 see page 5, line 15 - page 8, line 25 ---	1-3,6
X	EP 0 615 184 A (IBM) 14 September 1994 cited in the application see figures 1,2,15-19 see column 11, line 13 - column 13, line 3 -----	1-3,5,6

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Information on patent family members

International Application No

PCT/GB 97/00934

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2291991 A	07-02-96	WO 9712325 A	03-04-97
EP 0615184 A	14-09-94	JP 6274409 A	30-09-94